to heat treatment to form a semiconductor film having a crystal structure,

wherein a channel formation region is formed form the semiconductor film having the crystal structure, and

wherein the {101} plane in the semiconductor film having the crystal structure reaches 30% or more of all the lattice planes detected by Electron backscatter diffraction.

[Claim 20]

A method of manufacturing a semiconductor device according to any one of claims 16 to 19, wherein the thickness of the amorphous semiconductor film is 10 nm through 100 nm.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention pertains]

The present invention relates to a semiconductor film having a crystal structure and a method of manufacturing the semiconductor device whose active region is formed of this semiconductor film. In particular, the present invention is suitable for a method of manufacturing a thin film transistor formed a channel formation region in this semiconductor film. The term semiconductor device herein refers to a semiconductor device in general which utilizes semiconductor characteristics to function, and semiconductor integrated circuits, electro-optical devices, and electronic equipment mounted with the semiconductor integrated circuits or the electro-optical devices fall within this category.

[0002]

[Prior Art]

A technique has been developed for manufacturing a thin film transistor

(hereinafter referred to as TFT) from a semiconductor film that has a crystal structure (the film is hereinafter referred to as crystalline semiconductor film) and is formed on a glass, quarts or other substrate. A technique of forming a TFT from a crystalline semiconductor film is applied to flat panel displays, typically, liquid crystal display devices, as measures for realizing high definition image display, and is applied to monolithic displays in which a pixel portion and an integrated circuit necessary to drive the pixel portion are formed on the same substrate, as measures for realizing it.

[0003]

A known alternative to SOI (Silicon on Insulator Technology) in forming a crystalline semiconductor film is to use vapor growth method (CVD) in which a crystalline semiconductor film is formed by direct deposition on a substrate, or to crystallize an amorphous semiconductor film by heat treatment or laser light irradiation. However, the formed crystalline semiconductor film is to be applied to a TFT, the latter method is employed more often because the method provides the TFT with excellent electric characteristics.

[0004]

A crystalline semiconductor film can have a polycrystal structure if it is obtained by subjecting an amorphous semiconductor film formed on a glass, quarts or other substrate to heat treatment or laser light irradiation for crystallization. Crystallization is known to progress from a crystal nuclear spontaneously generated in the interface between the amorphous semiconductor film and the substrate. While crystal grains in a polycrystal structure each educe an arbitrary crystal plane, it has been found that the proportion, which the crystallization of the {111} plane requiring the minimum interface energy is educed, is high if silicon oxide is placed under the crystalline semiconductor film.

[0005]

Meanwhile, the thickness of a semiconductor film required for TFT is about 10 to 100 nm. However, it is difficult with in this thickness range to control crystal orientation in the interface between the semiconductor film and a substrate that is formed from a different material due to lattice discordance or crystal nuclei generated irregularly. Also, it has been impossible to increase the grain size of each crystal grain because of mutual interference between crystal grains.

[0006]

Another method of forming a crystalline silicon film has been disclosed in which an element for promoting crystallization of silicon is introduced into an amorphous silicon film, thereby obtaining a crystalline silicon film through heat treatment at a temperature lower than in prior art. For example, Japanese Patent Application Laid-open Nos. Hei 7-130652 and Hei 8-78329 describe obtaining a crystalline silicon film by introducing nickel or other metal element into an amorphous silicon film and subjecting the film to heat treatment at 550°C for four hours.

[0007]

In this case, the element introduced at a temperature lower than the temperature at which a natural nuclear is generated forms silicide, and crystal growth starts from this silicide. For instance, when the element is nickel, nickel silicide ($NiSi_x$ ($0.4 \leq x \leq 2.5$) is formed. While nickel silicide has no specific orientation, it advances crystal growth in an amorphous silicon film almost only in the direction parallel to the substrate if the thickness of the film is 10 to 100 nm. In this case, the interface energy of the interface between $NiSi_x$ and the {111} plane of the crystalline silicon is the smallest, and hence the plane parallel to the surface of the crystalline silicon film is the {110} plane to orient crystals mainly in the {110} plane orientation. However, when the crystal growth direction is parallel to the substrate surface and a crystal grows into a pillar, the crystal may not always

be oriented in the {110} plane orientation because there is a degree of freedom in the rotation direction as axis of the pillar-like crystal. Accordingly, other lattice planes are deposited.

[0008]

[Technical Problems before the Present Invention]

When the orientation ratio is low, continuity of lattices cannot be maintained in a crystal grain boundary where crystals of different orientations meet one another, resulting in formation of many dangling bonds. The dangling bonds formed in the crystal grain boundary acts as recombination center or trap center, to thereby lower the carrier (electrons or holes) transportation characteristic. As a result, carriers are lost in recombination or trapped by defects. If a crystalline semiconductor film as such is used to form a TFT, the TFT cannot have high electric field effect mobility.

[0009]

Also, controlling positions of crystal grains as desired is nearly impossible and crystal grain boundaries are placed irregularly, which does not allow a TFT to form its channel formation region solely from crystal grains of a specific crystal orientation. This lowers the continuity of crystal lattices and forms defects in crystal grain boundaries, thereby causing fluctuations in TFT characteristics and presenting various adverse influences. For instance, the field effect mobility is degraded to make the TFT incapable of operating at high speed. In addition, a fluctuation in threshold voltage is an obstruction to low voltage driving, leading to an increase in power consumption.

[0010]

The present invention has been made to present solutions to those problems, and an object of the present invention is therefore to raise the orientation ratio of a crystalline semiconductor film obtained by crystallizing an

amorphous semiconductor film through heat treatment and irradiation of intense light such as laser light, ultraviolet rays, or infrared rays and to provide a semiconductor device whose active region is formed from the crystalline semiconductor film and a method of manufacturing the semiconductor device.

[0011]

[Means for solving the Problem]

In order to solve the above problems, the present invention uses a semiconductor film containing silicon and germanium as its ingredient and having a crystal structure, the semiconductor film having the {101} plane that reaches 30% or more of all the lattice planes detected by reflection electron diffraction pattern method. This semiconductor film is obtained by forming an amorphous semiconductor film containing silicon and germanium as its ingredient through plasma CVD in which hydride, fluoride, or chloride gas of a silicon element is used, the repetition frequency is set to 10 kHz or less, and the duty ratio is set to 50% or less for intermittent electric discharge or pulsed electric discharge, and by introducing an element for promoting crystallization of this amorphous semiconductor film to the surface thereof to crystallize the amorphous semiconductor film through heat treatment, or through heat treatment and irradiation of intense light such as laser light, ultraviolet rays, or infrared rays, while utilizing the introduced element. The semiconductor film having a crystal structure can be used for an active layer such as a channel formation region.

[0012]

The thus formed semiconductor film containing silicon and germanium and having a crystal structure contains Group 14 elements in the periodic table other than silicon in a concentration of 1×10^{18} atoms/cm^3 or below. The semiconductor film contains less than 5×10^{18} nitrogen atoms per cm^3, less than 5×10^{18} carbon atoms per cm^3, and less than

1×10^{19} oxygen atoms per cm^3.

[0013]

The element for promoting crystallization is one or more elements selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, and Au. The thickness of the amorphous semiconductor film is set to 10 to 100 nm.

[0014]

[Embodiment Modes of the Invention]

The present invention is characterized in that a semiconductor film used for a channel formation region of a TFT is a crystalline semiconductor film having high {110} lattice plane orientation ratio and containing silicon and germanium as its ingredient. A typical embodiment mode of obtaining this crystalline semiconductor film includes: forming an amorphous semiconductor film containing silicon and germanium as its ingredient through plasma CVD by intermittent electric discharge or pulsed electric discharge in which hydride, fluoride, or chloride gas of a silicon atom and a germanium atom is used; introducing an element for promoting crystallization of the amorphous semiconductor film to the surface thereof; and crystallizing the amorphous semiconductor film through heat treatment, or through heat treatment and irradiation of intense light such as laser light, ultraviolet rays, or infrared rays, while utilizing the introduced element to form the crystalline semiconductor film.

[00015]

A substrate suitable for forming this crystalline semiconductor film is a non-alkaline glass substrate such as an aluminoborosilicate glass substrate and a barium borosilicate glass substrate. Typically, a Corning # 7059 glass substrate or a Corning # 1737 glass substrate (product of Corning Incorporated) is used. A quartz substrate or a sapphire substrate may also be used. Alternatively, a silicon, germanium, gallium, arsenic

or other semiconductor substrate with an insulating film formed on its surface may be used as the substrate.

[0016]

If the glass substrate is chosen, a blocking layer is formed between the amorphous semiconductor film and the glass substrate from silicon nitride, silicon oxide, silicon oxynitride or the like. The blocking layer prevents an impurity element such as an alkaline metal element contained in the glass substrate from diffusing into the semiconductor film. For example, a silicon nitride film is formed by plasma CVD using as reaction gas SiH_4, NH_3 and N_2. If a silicon oxynitride film is to be formed instead, SiH_4, N_2O and NH_3 are used as reaction gas. The blocking layer is formed to have a thickness of 20 to 200 nm.

[0017]

The amorphous semiconductor film is formed on the thus prepared substrate by plasma CVD using intermittent electric discharge or pulsed electric discharge. The intermittent electric discharge or pulsed electric discharge is obtained by modulating high frequency power with an oscillation frequency of 1 to 120 MHz, preferably 13.56 to 60 MHz, into power with a repetition frequency of 10 to 10 kHz and by supplying the modulated power to a cathode. When the duty ratio is defined as the ratio of time during which high frequency power application lasts in one cycle of the repetition frequency, the duty ratio is desirably set to 1 to 50%.

[0018]

One of the reasons for employing intermittent electric discharge or pulsed electric discharge as above is that it allows selection of radical species (meaning here atoms or molecules that are electrically neutral and chemically active) in the deposition process of the amorphous semiconductor film. For example, various radical species and ion species

are generated when dissolving SiH4 in an electric discharge space. When electric discharge is constituted steadily, the existence proportions of radical species keep fixed. On the other hand, if there is a period where electric discharge is turned off as in intermittent electric discharge or pulsed electric discharge, only radical species that has longer life period is supplied due to the difference in life period between the radical species and ion species to the film deposition surface and is used to form the film.

[0019]

Fig. 18 is a diagram schematically illustrating applying of high frequency power and changes with time in radical concentration. The intermittent electric discharge or pulsed electric discharge according to the present invention includes ON time in which high frequency power is applied to a cathode and OFF time in which the supply of high frequency power is shut off. For example, in the case where high frequency power having an oscillation frequency of 27 MHz is supplied at a repetition frequency of 10 kHz and a duty ratio of 10%, ON time is 1 μsec whereas OFF time is 9 μsec. Radical species and ion species generated by electric discharge are different from one another in generation speed and extinguishment speed (life period). If some radical species is picked out, the concentration of this radical species changes transiently as shown in Fig. 18. To elaborate, the concentration of the radical species increases as high frequency power is supplied until it reaches some saturation state. The radical species decreases and is extinguished when the supply of high frequency power is cut and its parent gas molecule is no longer dissociated. The extinguishment takes a certain period of time. Usually, the life period is defined as the time a radical species takes to decrease to 1/e.

[0020]

For example, SiH radical and SiH_2 radical have life periods of 1.72×10^{-4}, 2.47×10^{-6} seconds, respectively (these values are of when the radicals are in SiH_4 plasma at 50

mTorr). SiH_3 is considered by contrast as long-living from the fact that it repeats the $SiH_3 + SiH_4 \rightarrow SiH_3 + SiH_4$ reaction. It is said that SiH_3 is appropriate for forming an amorphous silicon film of excellent quality. GeH_4 is smaller in dissolution energy than SiH_4, and hence generates a large number of Ge radicals (or atomic-state Ge) when dissolved with the same high frequency power as SiH_4. The Ge radicals are presumably active and short-living.

[0021]

Accordingly, by optimizing the repetition frequency and the duty ratio, a given radical species can selectively be taken out to be used for film formation preemptively. In practice, a radical species having a long life period is taken out. A long-living radical species is low in chemical activity relatively, and hence it makes easy to control surface reaction in forming the film.

[0022]

Selection of radical species is reduced as the duty ratio becomes larger, making the film formation mechanism identical with the film formation mechanism in continuous electric discharge with no modulation. According to the experiments conducted by the present inventors, the effects provided by the intermittent electric discharge are decreased when the duty ratio exceeds 50%.

[0023]

In any case, the gas used in the present invention has to be refined to high purity in order to reduce the concentration of impurity elements such as oxygen, nitrogen, and carbon mixed in the amorphous semiconductor film during deposition. The amorphous semiconductor film formed by deposition has a thickness of 10 to 100 nm.

[0024]

The amorphous semiconductor film used in the present invention is formed from

a material containing silicon and germanium as its ingredients, and contains Group 14 elements other than silicon and germanium in a concentration of less than 5×10^{18} /cm^3. In forming this amorphous semiconductor film, typical reaction gas, namely, a mixture of SiH_4 and GeH_4, or SiH_4 and GeH_4 diluted by H_2 is used. SiH_4 may be replaced by Si_2H_6 or SiF_4 whereas GeH_4 may be replaced by GeF_4. Nitrogen, carbon, and oxygen, and their concentrations are less than 5×10^{18} /cm^3, less than 5×10^{18} /cm^3, and less than 1×10^{19} /cm^3, respectively, as the different kind elements contained in the amorphous semiconductor film. These impurities deposit mainly in grain boundaries of crystal grains during crystallization process and raise the potential barrier of the grain boundaries, thereby causing inconveniences such as impaired carrier mobility.

[0025]

Further, in the present invention the concentration of the different kind elements contained in the amorphous semiconductor film is herein detected by secondary ion mass spectroscopy (SIMS), and indicates the lowest concentration value in the film.

[0026]

An element for promoting crystallization of an amorphous semiconductor film is introduced to the thus formed amorphous semiconductor film. Examples of the element include one or more elements selected from the group consisting of iron (Fe), nickel (Ni), cobalt (Co), ruthenium (Ru), rhodium (Rh), palladium (Pd), osmium (Os), iridium (Ir), platinum (Pt), copper (Cu), and gold (Au). The elements listed above can be used as the element for promoting crystallization of the amorphous semiconductor film in every mode of the present invention which is described in this specification. The above elements all provide the same effect at the same level, though nickel is the element that is typically used.

[0027]

The elements are introduced to the entire surface of the amorphous

semiconductor film, or to the surface of the amorphous semiconductor film of slits or dots state suitably placed. In the former case, the surface of the amorphous semiconductor film to which the elements are to be introduced may be the substrate side surface or the surface opposite to the substrate. In the latter case, an insulating film is preferably formed on the amorphous semiconductor film so that the elements are introduced to the amorphous semiconductor film through openings formed in the insulating film. The size of the openings is not particularly limited, but a recommended width is 10 to 40 μm. The longitudinal length of the openings may be set to an arbitrary value within a range of several tens μm to several tens cm.

[0028]

The method of introducing the elements is not particularly limited as long as the method such as elements are held to the surface of the amorphous semiconductor film or the elements are mixed into the amorphous semiconductor film. Examples of the usable introduction method include sputtering, evaporation, plasma treatment (including plasma CVD), adsorption, and application of a metallic salt solution. In plasma treatment, the elements sputtered from the cathode in a glow electric discharge atmosphere by inert gas are used. Application of a metallic salt solution is easy, and advantageous as regard the simpleness of adjusting the elements concentration.

[0029]

Various kinds of salts can be used for the metallic salt. Examples of the usable solvent include water; alcohols, aldehyde esters, ethers or other organic solvents; and a mixture of water and these organic solvents. The metallic salt may not always be dissolved completely in the solution. A solution in which a part of or the entirety of metallic salt is suspended may be used. Whatever method is employed, the elements have to be introduced to the surface of the amorphous semiconductor film or into the amorphous

semiconductor film while being dispersed.

[0030]

After the elements are introduced by one of the above methods, the amorphous semiconductor film is crystallized utilizing the introduced elements. The crystallization is achieved by heat treatment or by irradiating the film with intense light such as laser light, ultraviolet rays, and infrared rays (hereinafter collectively referred to as laser treatment). Heat treatment alone can provide a crystalline semiconductor film in which the major orientation is the {101} plane orientation. However, heat treatment is preferably followed by irradiation of intense light such as laser light. The laser treatment subsequent to the heat treatment can repair crystal defects left in crystal grains, and hence is an effective measure to improve the quality of crystals formed.

[0031]

The temperature in the heat treatment can range from 450 to 1000°C. One probable upper limit for the temperature is set by the heat resistance of the substrate used. For example, a quartz substrate can withstand heat treatment at 1000°C. On the other hand, in the case of a glass substrate, one probable upper limit for the temperature can be set based on the distortion point of the glass substrate so as to be lower than the same. For example, when the glass substrate has a distortion point of 667°C, an appropriate upper temperature limit will be about 660°C, preferably 600°C or less. The time required for the heat treatment slightly varies depending upon the heating temperature and conditions for the subsequent treatment (e.g., whether or not laser light irradiation treatment is carried out). Preferably, the heat treatment is conducted at 550 to 600°C for four to twenty-four hours. If the heat treatment is followed by laser treatment, the heat treatment is conducted at 500 to 550°C for four to eight hours. The above heat treatment may be conducted in air or a hydrogen atmosphere, preferably, a nitrogen atmosphere or an inert gas atmosphere.

[0032]

The laser treatment uses as a light source an excimer laser having a wavelength of 400 nm or less, or the second harmonic (wavelength: 532 nm) to the fourth harmonic (wavelength: 266 nm) of a YAG laser or of a YVO_4 laser. These laser lights are collected by an optical system into linear beam or spot light. The energy density of the laser light upon irradiation is set to 100 to 300 mJ/cm^2. The collected laser beam such as the above is run over a given region of the substrate to process the region. Instead of the laser, a halogen lamp, a xenon lamp, a mercury lamp, a metal halide lamp, etc. may be used as the light source.

[0033]

The model capable of obtaining, through the above steps, the crystalline semiconductor film of the present invention in which the ratio of the {101} plane orientation is high can be inferred roughly as follows. The inference will be described with reference to Fig. 19.

[0034]

An element for promoting crystallization of silicon is introduced into an amorphous semiconductor film 2402 formed on a substrate 2401, and quickly diffuses into the amorphous semiconductor film 2402 during dehydrogenation treatment. Then the element and silicon react to each other to form a silicide 2403. The silicide serves as a crystal nuclear to start crystal growth later. For instance, nickel used as a typical element forms $NiSi_x$. Since solid germanium is hardly dissolve into $NiSi_x$, $NiSi_x$ in the amorphous semiconductor film 2402 moves while pushing germanium aside.

[0035]

$NiSi_x$ does not have particular orientation. However, when the amorphous semiconductor film has a thickness of 10 to 100 nm, $NiSi_x$ can grow almost only in the

direction parallel to the substrate surface. In this case, the interface energy of the interface between $NiSi_x$ and the {111} plane of the crystalline silicon is the smallest, and hence the plane parallel to the surface of the crystalline silicon film is the {110} plane to orient crystals mainly in the {110} plane orientation. However, when the crystal growth direction is parallel to the substrate surface and a crystal grows into a pillar, the crystal may not always be oriented in the {110} plane orientation because there is a degree of freedom in the rotation direction as axis of the pillar-like crystal. Accordingly, other lattice planes are deposited.

[0036]

From the viewpoint of $NiSi_x$, germanium having a large atom radius is present only in portions of amorphous semiconductor film which surround $NiSi_x$, and it is expected that a great distortion (tensile stress) is generated. Because of this distortion energy, the critical radius of nuclear generation is increased. Furthermore, the distortion (tensile stress) presumably has an effect of limiting crystal orientation of $NiSi_x$ nuclei and enhancing the orientation ratio of a specific crystal plane ({101} plane, to be exact).

[0037]

The structure of $NiSi_x$ is of fluorite, where a nickel atom is arranged between silicon lattices having the diamond structure. When the nickel atom is removed from $NiSi_x$, the silicon crystal structure is left. From the results of numerous experiments, it has been found that the nickel atom moves toward the amorphous silicon side. Supposedly, this is because the solid solution rate is higher in the amorphous silicon than in the crystalline silicon. Accordingly, a model is proposed in which formation of a crystalline silicon film 2404 seems to advance as nickel moves in the amorphous silicon.

[0038]

In order to enhance the ratio of the {101} plane orientation in the crystalline

semiconductor film, an amorphous semiconductor film composed of silicon and germanium is doped with an element for promoting crystallization of silicon and crystallized by heat treatment and laser treatment in the present invention.

[0039]

The present inventors have found that the crystal nuclear generation density is lowered when an amorphous semiconductor film, specifically, an amorphous silicon film, contains 0.1 to 10 atomic percent of germanium. Fig. 20 is a result of studying the GeH_4 dose dependency in relation to the distance between adjacent crystal nuclei. The axis of ordinate shows the cumulative frequency. As film formation conditions, the sum flow rate of GeH_4 diluted by SiH_4 and hydrogen to 10% is set to a constant value, 100 SCCM.

[0040]

Fig. 20A shows results when an aqueous solution containing 3 ppm of nickel acetate is used as the element for promoting crystallization of silicon, whereas Fig. 20B shows results of 1 ppm. An increase in GeH_4 dose means an accompanying increase in concentration of germanium contained in the amorphous silicon film as the GeH_4 dose increase. The results in Figs. 20A and 20B both show that the distance between adjacent crystal nuclei is longer when the GeH_4 dose is larger. Fig. 21 shows crystal nuclear density in relation to GeH_4 dose based on the results. It can be read that the crystal nuclear density decreases as the GeH_4 dose increases.

[0041]

From the standpoint of nuclear generation theory, an energy change ΔG when a nuclear having a volume V appears in the parent phase is given by the following equation.

[0042]

[Equation 1]

$$\Delta G=\Delta GvXV+EXV+\gamma sXS$$

[0043]

Wherein, ΔGv represents a free energy change (negative) per unit volume, the first term in the right side member represents driving force of nuclear generation, whereas E represents a distortion energy per unit volume, γs represents an interface energy per unit volume (S is a surface area of a nuclear deposited), and the second and third terms represent forces that work against deposition of nuclei. Because of these two terms, a nuclear having a critical radius of r_0 or less is unstable in terms of energy (ΔG increases together with r) and is eventually extinguished if generated at all. In other words, the equation shows that only nuclei having a critical radius of larger than r_0 are stable. This confirms that the presence of germanium in an amorphous silicon film works to increase the critical radius in nuclear generation in the above speculation.

[0044]

Then, regarding to a crystalline semiconductor film which is formed based on the above present invention, an example of a condition for manufacturing is shown. A chart 1 is the condition for manufacturing of the amorphous semiconductor film by the plasma CVD. GeH_4 diluted by SiH_4 and hydrogen to 10% is used for the reaction gas. In order to reduce the concentration of impurities such as oxygen, nitrogen, and carbon included in the amorphous semiconductor film to be formed, SiH_4 of 99.9999% or higher purity and highly pure GeH_4 containing 1 ppm or less of nitrogen, 1 ppm or less of hydrocarbon compound, and 2 ppm or less of CO_2 are used for the reaction gas. High frequency power supply a peak at 0.35 W/cm^2 (27 MHz) and is modulated into pulsed electric discharge with a repetition frequency of 1 to 30 kHz and a duty ratio of 10 to 90% to be supplied to a cathode of a parallel flat type plasma CVD apparatus. Other conditions include setting the reaction pressure to 33.25 Pa, the substrate temperature to 200 to 400°C, and the distance between electrodes to 35 mm.

[0045]

Fig. 17 is a picture taken during oscilloscope observation of the waveform of 27 MHz high frequency power applied to a cathode of a plasma CVD apparatus. Fig. 17A shows the case in which the repetition frequency is 1 kHz and the duty ratio is 20% whereas Fig. 17B shows the case in which the repetition frequency is 1 kHz and the duty ratio is 50%. As shown in the pictures, the amorphous semiconductor film according to the present invention is formed while alternating ON time in which high frequency power is applied with OFF time in which high frequency power is not applied. The electric discharge obtained by such mode of power supply is called intermittent electric discharge or pulsed electric discharge for conveniences' sake in this specification.

[0046]

Fig. 4 shows an example of a plasma CVD apparatus. A common chamber 1120 is connected to loading · unloading (L/UL) chambers 1110 and 1115, reaction chambers (1) to (3) 1111 to 1113, and a preliminary chamber 1114 via gate valves 1122 to 1127. Substrates are mounted to cassettes 1128 and 1129 of the loading · unloading (L/UL) chambers 1110 and 1115 and transported to the reaction chambers or to the preliminary chamber by transferring means 1121 of the common chamber 1120. The preliminary chamber 1114 is mainly only for preliminary heating of a substrate. The reaction chamber (1) is for forming an insulating film such as a silicon nitride film and a silicon oxide film. The reaction chamber (2) is for forming an amorphous semiconductor film. The reaction chamber (3) is for plasma treatment by which the film is doped with an element for promoting crystallization of silicon. The chambers are thus separated to work their respective works. In the plasma treatment, the element is sputtered from a cathode comprising the element for promoting crystallization, e.g., nickel by glow electric discharge of inert gas to adhere to the amorphous semiconductor film. A plasma CVD apparatus

structured as above can successively process formation of a blocking layer, which is to be formed contacting closely to a substrate, formation of an amorphous semiconductor film, and doping of an element for promoting crystallization of the amorphous semiconductor film, without exposing the device to the air.

[0047]

Fig. 5 illustrates in detail the structure of one of reaction chambers of a plasma CVD apparatus as above. The reaction chamber illustrated as an example is one for forming an amorphous semiconductor film. A reaction chamber 501 is of parallel flat type and is provided with a cathode 502 connected to a high frequency power 505, and an anode 503. The cathode 502 is a shower plate through which reaction gas is supplied to the reaction chamber from gas supplying means 506. The anode 503 is provided with heating means such as a sheathed heater, and a substrate 515 is placed on top. Details of the gas supplying system are omitted here but, to describe it briefly, the system is composed of a cylinder 514, a mass flow controller 512, a stop valve 513, and the like. The cylinder 514 is filled with SiH_4, GeH_4, or other gas, and the mass flow controller 512 controls the flow rate of the gas. Exhaust means 507 is composed of a gate valve 508, an automatic pressure control valve 509, a turbomolecular pump (or a compound molecular pump) 510, and a dry pump 507. The turbo molecular pump (or a compound molecular pump) 510 and the dry pump 507 do not use grease to completely eliminate the possibility of staining the reaction chamber with spattered oil. The reaction chamber has a volume of 13 L. The turbomolecular pump has an exhaust rate of 300 L/sec and is provided on the first stage of the reaction chamber whereas the dry pump has an exhaust rate of 40 m^3/hr and is provided on the second stage of the reaction chamber so as to prevent reverse diffusion of evaporated organic material from the exhaust system side. The pumps also enhance the attained vacuum in the reaction chamber and as prevent as possible impurity element from mixing in

the amorphous semiconductor film during its formation.

[0048]

Using an amorphous semiconductor film formed under the above conditions, the orientation ratio of the crystalline semiconductor film formed by the above crystallization method is obtained by electron backscatter diffraction pattern (EBSP). EBSP is a method of analyzing the crystal orientation from backscatter of the primary electron by setting a dedicated detector in a scanning electron microscope (SEM) (hereinafter this method is called an EBSP method for conveniences' sake). An estimation of a crystalline semiconductor film employing EBSP can be found in "Microtexture Analysis of Location Controlled Large Si Grain Formed by Exciter-Laser Crystallization Method", R. Ishihara and P. F. A. Alkemade, AMLCD '99 Digest of Technical Papers, 1999, Tokyo, Japan, PP. 99-102.

[0049]

In this measurement method, if an electron beam enters the sample having a crystal structure, inelastic scattering takes place also in the rear. There can also be observed a linear pattern peculiar to the crystal orientation by Bragg diffraction of the sample in inelastic scattering (the pattern is commonly called a Kikuchi image). The EBSP method obtains the crystal orientation of the sample by analyzing the Kikuchi image projected onto the screen of the detector. Information of the crystal direction or orientation can be obtained for a planar sample by the mapping measurement in which the point which hit the electron beam on the sample is moved along and the orientation analysis is repeated as the point is moved. The thickness of the incident electron beam varies depending on the type of the electron gun attached to the scanning electron microscope. In the case of the Schottoky electric field discharge type, the gun emits a very thin electron beam with a diameter of 10 to 20 nm. The mapping measurement can provide more averaged

information of the crystal orientation when the number of measurement points is greater and the area of the measurement range is wider. In a practical measurement, an area of 100 x 100 μm^2 is measured at about 10000 points (1 μm distance) to 40000 points (0.5 μm distance).

[0050]

When the crystal direction is obtained for all of the crystal grains by the mapping measurement, the crystal orientation state relative to the film can be expressed statistically. Fig. 6A shows an example of reverse pole diagram obtained by the EBSP method. A reverse pole diagram is often used when the major orientation of a polycrystal is shown, and it collectively illustrates which lattice plane coincides with a specific face of the sample (here, the film surface).

[0051]

The fan-shaped frame in Fig. 6A is the one generally called a standard triangle in which all indexes related to the cubic system are included. In this Fig, the length corresponds to the angle in the crystal direction. For instance, the distance between {001} and {101} is 45°, the distance between {101} and {111} is 35.26°, and the distance between {111} and {001} is 54.74°. The white dotted lines respectively indicate a range of offset angle of 5° and a range of offset angle of 10° from {101}.

[0052]

Fig. 6A is obtained by plotting all of the measurement points (11655 points in this example) in the mapping measurement onto the standard triangle. The points are dense in the vicinity of {101}. Fig. 6B translates concentration of points into contour. When assuming that the orientation of crystal grains is completely random, namely, when the points are evenly distributed throughout the standard triangle, the numeric values here show magnification and are dimensionless numbers.

[0053]

If it is found that there is the major orientation toward a specific index (here, {101}), the level of the major orientation is easy to image when the quantity of crystal grains centered around the specific index is expressed in numeric values. For example, the orientation ratio is expressed by and obtained from the following equation when the orientation ratio is given as the ratio of the points present in the range of offset angle of 5° and the range of offset angle of 10° from {101} to the whole points in the reverse pole diagram of Fig. 6A shown as an example (the ranges are indicated by the white dotted lines in the Fig.).

[0054]

[Equation 2]

$$\{101\}\ \text{orientation ratio} = \frac{\text{The number of measurement points in a range of an angle which is made by \{101\} lattice plane and a surface of a film and which is within an acceptable value}}{\text{All numbers of the measurement points}}$$

[0055]

Alternatively, this ratio can be described as follows. When the points are distributed heavily around {101} as in Fig. 6A, it is expected in the actual film that although the {101} orientation of the respective crystal grains is substantially perpendicular to the substrate the {101} orientation is arranged with some fluctuation. The acceptable angle for the fluctuation angle is 5° and 10°. Then the number of crystal grains whose {101} orientation is smaller than the acceptable angle is counted to express the ratio of them in numeric values. The orientation ratio can be obtained by setting the acceptable offset angles to 5° and 10° and calculating the ratio of crystal grains that fall within the acceptable

ranges as described above.

[0056]

Fig. 1 shows the {101} plane orientation ratio of a crystalline semiconductor film as the duty ratio dependency in intermittent electric discharge. The crystalline semiconductor film is obtained by forming an amorphous semiconductor film with a thickness of 54 nm on a quartz substrate based on the above formation conditions, and by subjecting the film to dehydrogenation treatment at 500°C for an hour and then by heating at 580°C for four hours. The repetition frequency is set to 10 kHz. It can clearly be read from Fig. 1 that the {101} plane orientation ratio increases when the duty ratio is 60% or less. According to the results in Fig. 1, the orientation ratio is 58% when the duty ratio is 30%.

[0057]

Fig. 2 shows data obtained by plotting the {101} plane orientation ratio while placing the repetition frequency in intermittent electric discharge on the axis of abscissa. The repetition frequency changes from 5 to 30 kHz. As the repetition frequency gets smaller, the {101} plane orientation ratio increases.

[0058]

Fig. 3 shows the reaction pressure dependency during formation of an amorphous semiconductor film. The {101} plane orientation ratio is raised as the pressure is lowered.

[0059]

Needless to say, such crystalline semiconductor film exhibiting high orientation with respect to {101} lattice plane is attained not only by deposing an amorphous semiconductor film utilizing setting the repetition frequency, the duty ratio, and the reaction pressure, but also by a synergetic effect of setting the concentration of oxygen, nitrogen, and

carbon contained in the film to less than 1 x 10^{19} /cm^3 and setting the thickness of the film to 20 to 100 nm to make the crystal growth in the direction parallel to the substrate surface dominant.

[0060]

Such a crystalline semiconductor film having high {101} lattice plane orientation ratio is suitable for a channel formation region that determines characteristics of an element, such as a channel formation region of a TFT and a photo-electric conversion layer of a photo-electromotive force element.

[0061]

[Embodiment]

[Embodiment 1]

Fig 7 illustrates a method of forming a crystalline semiconductor film in which an amorphous silicon film containing germanium is crystallized by doping the entire surface of the film with a metal element for promoting crystallization of silicon. In Fig. 7A, a substrate 101 is a glass substrate typical example of which is a Corning # 1773 glass substrate. A blocking layer 102 is formed on the surface of the substrate 101 from a silicon oxynitride film with a thickness of 100 nm by plasma CVD using SiH_4 and N_2O. The blocking layer 102 is provided in order to prevent an alkaline metal contained in the glass substrate from diffusing into a semiconductor film to be formed on the layer.

[0062]

An amorphous semiconductor film 103 comprised of silicon and germanium is formed by plasma CVD. GeH_4 gas diluted by SiH_4 and H_2 to 10% is introduced in a reaction chamber and dissolved by glow electric discharge to be deposited on the substrate 101. Details of the conditions thereof are as described in Embodiment Mode. Here, the amorphous semiconductor film 103 is deposited to a thickness of 54 nm through intermittent

electric discharge in which 27 MHz high frequency power is modulated, the repetition frequency is set to 5 kHz, and the duty ratio is set to 20%. The mixing ratio of SiH_4 and GeH_4 is adjusted so that the germanium concentration in the amorphous semiconductor to be formed is 1 to 10 atomic percent, preferably 2 to 3 atomic percent. In order to reduce impurities such as oxygen, nitrogen, and carbon in the amorphous semiconductor film 103 comprised of silicon and germanium as much as possible, SiH_4 gas of 99.9999% or higher purity and GeH_4 gas of 99.99% or higher purity are used. According to specifications of the plasma CVD apparatus to be used, the reaction chamber has a volume of 13 L. A compound molecular pump having an exhaust rate of 300 Ll/sec is provided on the first stage of the reaction chamber and a dry pump having an exhaust rate of 40 m^3/hr is provided on the second stage of the reaction chamber so as to prevent reverse diffusion of evaporated organic material from the exhaust system side. The pumps also enhance the attained vacuum in the reaction chamber to let the least possible amount of impurity element mix in the amorphous semiconductor film during its formation.

[0063]

Then, as shown in Fig. 7B, a nickel acetate solution containing 10 ppm of nickel by weight is applied by spinner to form a nickel containing layer 104. In order to make sure the solution permeates the film well, the surface of the amorphous semiconductor film 103 comprised of silicon and germanium is treated. As the surface treatment, a very thin oxide film is formed using an aqueous solution containing ozone, the oxide film is etched using a mixture of hydrofluoric acid and hydrogen peroxide to form a clean surface, and a very thin oxide film is again formed by treatment using an aqueous solution containing ozone. With the oxide film formed as above, the nickel acetate solution can be applied uniformly to the silicon surface, which is inherently hydrophobic.

[0064]

Next, heat treatment is conducted at 500°C for an hour so that hydrogen is released from the amorphous semiconductor film comprised of silicon and germanium. Then the film is subjected to another heat treatment at 580°C for four hours to crystallize the film. Thus a crystalline semiconductor film 205 shown in Fig. 7C is formed.

[0065]

In order to enhance the crystallization ratio (the ratio of crystalline components to the total volume of the film) and repair defects remaining in crystal grains, the crystalline semiconductor film 205 is subjected to laser treatment in which the film is irradiated with laser light 206. The laser used is an excimer laser having a wavelength of 308 nm and oscillating at 30 Hz. The laser light is collected by an optical system into a beam of 100 to 300 mJ/cm^2, and laser treatment is conducted with the overlapping ratio set to 90 to 95% without melting the semiconductor film. Thus a crystalline semiconductor film 107 comprised of silicon and germanium, which is shown in Fig. 7D, can be obtained.

[0066]

[Embodiment 2]

A method of selectively introducing an element for promoting crystallization of an amorphous semiconductor film will be described with reference to Fig. 8. In Fig. 8A, a substrate 120 may be the aforementioned glass substrate or a quartz substrate. When the glass substrate is employed, a blocking layer is formed as in Embodiment 1.

[0067]

An amorphous semiconductor film 121 comprised of silicon and germanium is formed by plasma CVD using intermittent electric discharge or pulsed electric discharge as in Embodiment 1.

[0068]

A silicon oxide film 122 with a thickness of 150 nm is formed on the amorphous

semiconductor film 121 comprised of silicon and germanium. The method of forming the silicon oxide film is not limited. For example, the film is formed through electric discharge in which a mixture of tetraethyl ortho silicate (TEOS) and O_2 is used, the reaction pressure is set to 40 Pa, the substrate temperature is set to 300 to 400°C, and the high frequency (13.56 MHz) power density is set to 0.5 to 0.8 W/cm^2.

[0069]

Next, an opening 123 is formed in the silicon oxide film 122 and a nickel acetate solution containing 10 ppm of nickel by weight is applied to the film. A nickel containing layer 124 is thus formed and the only part of the nickel containing layer 124 that is in contact with the amorphous semiconductor film 121 is at the bottom of the opening 123.

[0070]

In Fig. 8B, the film is crystallized by heat treatment at 500 to 650°C for four to twenty-four hours, for example, at 570°C for fourteen hours. In this case, a part of the amorphous silicon film that is in contact with nickel is crystallized first and the crystallization advances from that part in the direction parallel to the substrate surface. A crystalline silicon film 125 is thus formed. The crystalline silicon film 125 is masses of rod-like or needle-like crystals, and each crystal grows with a specific directivity when viewed macroscopically. The silicon oxide film 222 is then removed to complete the crystalline semiconductor film 225 comprised of silicon and germanium, which is shown in Fig. 8C.

[0071]

[Embodiment 3]

The crystalline semiconductor film formed in accordance with the method described in Embodiment 1 or 2 still has the element that has been utilized in crystallization, typically, nickel. Although not distributed in the film uniformly, the element remains in a

concentration over 1 x 10^{19} atoms/cm^3 on the average. The film in this state can be used for a TFT and a channel formation region of other various semiconductor devices, of course, but it is preferred to remove the element from the film by gettering.

[0072]

This embodiment describes an example of the gettering method with reference to Fig. 9. In Fig. 9A, the glass substrate of Embodiment 1 or a quartz substrate is employed as a substrate 130. When the glass substrate is used, a blocking layer is formed similar to Embodiment 1. A crystalline semiconductor film 131 is formed by the method described in Embodiment 1 or the method described in Embodiment 2. On the surface of the crystalline semiconductor film 131, a silicon oxide film 132 to serve as a mask is formed to a thickness of 150 nm. An opening 133 is formed in the silicon oxide film to expose a part of the crystalline semiconductor film. If the film is formed in accordance with Embodiment 2, the silicon oxide film 122 shown in Fig. 8A can be used for the film 132 as it is, proceeding to the step of this embodiment after the step of Fig. 8B is completed. Then the film is doped with phosphorus by ion doping to form a phosphorus-doped region 135 that contains phosphorus in a concentration of 1 x 10^{19} to 1 x 10^{22} /cm^3.

[0073]

Thereafter, heat treatment is conducted in a nitrogen atmosphere at 550 to 800°C for five to twenty-four hours, for example, at 600°C for twelve hours. Through the heat treatment, the phosphorus-doped region 135 works as a gettering site and the catalytic element remained in the crystalline semiconductor film 131 is segregated in the phosphorus-doped region 135.

[0074]

After that, the silicon oxide film 132 that has served as a mask and the phosphorus-doped region 135 are removed by etching as shown in Fig. 9C. Thus obtained

is a crystalline semiconductor film 136 in which the concentration of the metal element used in the crystallization step is reduced to less than 1×10^{17} /cm^3.

[0075]

[Embodiment 4]

Now, a description will be given on an example of manufacturing a TFT from the crystalline semiconductor film comprised of silicon and germanium as above. Fig. 11 is a diagram illustrating the manufacturing process of this embodiment.

[0076]

In Fig. 11A, a crystalline semiconductor film 212 comprised of silicon and germanium is formed on a substrate 210. As the crystalline semiconductor film 212, a crystalline semiconductor film formed in accordance with one of the methods of Embodiments 1 to 3 is employed. In manufacturing a TFT from the film, the film is etched and divided into island-like films having given sizes in order to separate elements. When the substrate 210 is a glass substrate, a blocking layer 211 is formed.

[0077]

An insulating film 213 to be utilized as a gate insulating film in the TFT is formed to a thickness of 30 to 200 nm. The insulating film 213 is a silicon oxynitride film formed by plasma CVD from SiH_4 and N_2O, or a silicon oxynitride film formed from TEOS and N_2O by plasma CVD. In this embodiment, the former film is chosen and the thickness thereof is set to 70 nm.

[0078]

On the insulating film 213, a gate electrode 214 is formed from a conductive material composed of one or more elements selected from the group consisting of tantalum, tungsten, titanium, aluminum and molybdenum.

[0079]

Thereafter, an impurity region 216 having one conductivity type is formed as shown in Fig. 11B for forming a source and drain region of the TFT. The impurity region 216 is formed by ion doping. The film is doped with a Group 15 element in the periodic table, typically, phosphorus or arsenic, if an n-channel TFT is to be manufactured, whereas a Group 13 element in the periodic table, typically, boron, is used for the doping if it is a p-channel TFT that is to be manufactured.

[0080]

A first interlayer insulating film 817 is then formed using a silicon nitride film or a silicon oxynitride film formed by plasma CVD. The first interlayer insulating film 817 is formed by plasma CVD while setting the substrate temperature at 200 to 300°C, and then is subjected to heat treatment in a nitrogen atmosphere at 350 to 450°C, preferably 410°C. At this temperature, hydrogen is released from the first interlayer insulating film. Thereafter, another heat treatment is performed at 250 to 350°C, lasting about 0.1 to 1 hour to hydrogenate the crystalline semiconductor film. Hydrogenating the crystalline semiconductor film through two-step heat treatment as above makes it possible to hydrogenate and compensate dangling bonds (uncoupled bonds) of germanium, which is difficult to hydrogenate especially at a temperature of 350°C or higher. A source and drain electrode 218 is then formed to complete the TFT.

[0081]

Although the TFT shown here has a single gate structure, the TFT may of course take a multi-gate structure in which a plurality of gate electrodes are provided.

[0082]

The crystalline semiconductor film comprised of silicon and germanium and obtained by the present invention has high {101} plane orientation ratio and can form a channel formation region that shows excellent interface characteristics regarding the

interface with the gate insulating film. The crystalline semiconductor film is also low in defect density in crystal grain boundaries and inside crystal grains, and can provide high electric field effect mobility. The description here is given with the TFT having a single drain structure. However, a TFT having a lightly doped drain (LDD) structure or a TFT in which an LDD region overlaps a gate electrode can also be formed. The TFT fabricated in accordance with the present invention can be used as a TFT for manufacturing an active matrix liquid crystal display device or EL display device, or as a TFT constituting a thin film integrated circuit that is to replace the conventional LSI formed from a semiconductor substrate.

[0083]

[Embodiment 5]

Fig. 10 is a sectional view of a reverse stagger TFT manufactured from a crystalline semiconductor film composed of silicon and germanium in accordance with the present invention. In the reverse stager TFT, gate electrodes 260, 261 are formed on a glass or quartz substrate 201, and crystalline semiconductor films 263, 264 containing silicon and germanium as their ingredients are formed on a gate insulating film 262. The crystalline semiconductor films 263, 264 may be any of the crystalline semiconductor films formed in accordance with the methods of Embodiments 1 through 3.

[0084]

An n-channel TFT 280 is formed from the crystalline semiconductor film 263, and has a channel formation region 273, an LDD region 274 that is formed by doping of an n-type impurity element (donor), and a source or drain region 275. A p-channel TFT 281 is formed from the crystalline semiconductor film 264, and has a channel formation region 276 and a source or drain region 277 formed by doping of a p type impurity element (acceptor).

[0085]

Channel protective films 265, 266 are formed on the channel formation regions 273, 276, respectively. Source or drain electrodes 269 to 272 are formed through a first interlayer insulating film 267 and a second interlayer insulating film 268. The first interlayer insulating film 267 is formed from a silicon nitride film or a silicon oxynitride film. Thereafter, the film is subjected to heat treatment in an nitrogen atmosphere at 350 to 450°C, preferably 410°C. At this temperature, hydrogen is released from the first interlayer insulating film. Then another heat treatment is performed at 250 to 350°C, lasting about 0.1 to 1 hour to hydrogenate the crystalline semiconductor film.

[0086]

A reverse stagger TFT as above also can construct a driver circuit of an active matrix liquid crystal display device or EL display device. Other than the driver circuit, an n-channel TFT or a p-channel TFT as the one described above can be applied to a transistor constituting a pixel portion. Although the TFT shown here has a single gate structure, the TFT may of course take a multi-gate structure in which a plurality of gate electrodes are provided. The TFT of this embodiment can be used as a TFT constituting a thin film integrated circuit that is to replace the conventional LSI formed from a semiconductor substrate.

[0087]

[Embodiment 6]

A description given in this embodiment with reference to Fig. 12 is about an example of manufacturing a CMOS TFT obtained by combining an n-channel TFT and a p-channel TFT complementarily. In Fig. 12A, a crystalline semiconductor film composed of silicon and germanium is formed on a substrate 301. The crystalline semiconductor film may be any one of crystalline semiconductor films formed in accordance with the methods

of Embodiments 1 through 3. In manufacturing a TFT from the film, the film is etched and divided into island-like semiconductor films 331 to 333 having given sizes in order to separate elements. When the substrate 301 is a glass substrate, a blocking layer 302 is formed.

[0088]

For the blocking layer 302, a silicon oxynitride film is formed by plasma CVD using SiH_4 and N_2O to a thickness of 50 to 200 nm. Alternatively, the blocking layer may have a two-layer structure in which a silicon oxynitride film formed from SiH_4, NH_3 and N_2O by plasma CVD to a thickness of 50 nm and a silicon oxynitride film formed from SiH_4 and N_2O to a thickness of 100 nm are layered. The two-layer structure may instead be obtained by layering a silicon nitride film and a silicon oxide film that is formed using TEOS (Tetraethyl Ortho Sillicate).

[0089]

The blocking layer 302 and an amorphous semiconductor film to be formed on the blocking layer may both be formed by plasma CVD. Therefore these layers can be formed in succession in the same reaction chamber of a single chamber CVD apparatus, or in a multi-chamber CVD apparatus where the substrate is moved from one reaction chamber to another reaction chamber. In either case, the blocking layer and the amorphous semiconductor film are formed without being exposed to the air, thereby keeping the interface between the two clean.

[0090]

An insulating film 334 to be utilized as a gate insulating film is formed by plasma CVD or sputtering to a thickness of 40 to 150 nm. In this embodiment, a silicon oxynitride film with a thickness of 70 nm is formed. A material particularly preferable as the gate insulating film is a silicon oxynitride film formed from SiH_4 and N_2O added with

O_2, for the fixed charge density in this film is low. The gate insulating film is not limited to the silicon oxynitride film given above, of course, but it may be a single layer of insulating film such as a silicon oxide film and a tantalum oxide film, or a laminate of those insulating films.

[0091]

A first conductive film 335 and a second conductive film 336 for forming gate electrodes are formed on the insulating film 334. In this embodiment, the first conductive film 335 is a tantalum nitride film or a titanium film with a thickness of 50 to 100 nm whereas the second conductive film 336 is a tungsten film with a thickness of 100 to 300 nm. These materials are stable in heat treatment conducted in a nitrogen atmosphere at 400 to 600°C, and do not increase the resistivity much.

[0092]

Next, a resist mask 337 is formed as shown in Fig. 12B to conduct first etching treatment for forming the gate electrodes. The etching method is not limited to a particular method but, preferably, the ICP (Inductively Coupled Plasma) etching is employed. In the etching treatment, CF_4 and Cl_2 are mixed as etching gas, and plasma is generated by giving RF (13.56 MHz) power of 500 W to a coiled electrode at a pressure of 0.5 to 2 Pa, preferably 1 Pa. RF (13.56 MHz) power of 100 W is also given to the substrate side (sample stage) so that substantially negative self-bias voltage can be applied. In the case where mixture of CF_4 and Cl_2 is used, the tungsten film and the tantalum nitride film or the titanium film are etched at almost the same rate.

[0093]

Under the etching conditions given in the above, the edges of the films can be tapered by the shape of the resist mask and the effect of the bias voltage applied to the substrate side. The angle of the tapered portion is set to 15 to 45°. In order to etch the

films without leaving any residue on the gate insulating film, the etching time is prolonged by about 10 to 20%. The selective ratio of the silicon oxynitride film to the W film is 2 to 4 (typically, 3), and hence the exposed surface of the silicon oxynitride film is etched by about 20 to 50 nm through the over-etching treatment. Through the first etching treatment, first shape conductive layers 338 to 340 (first conductive layers 338a to 340a and second conductive layers 338b to 340b) are formed from the first conductive film and the second conductive film. Denoted by 341 is a gate insulating film and a region of the gate insulating film which is not covered with the first shape conductive layers is etched and thinned by about 20 to 50 nm.

[0094]

Second etching treatment is then conducted as shown in Fig. 12C. In this etching treatment, ICP etching is employed, CF_4, Cl_2 and O_2 are mixed as etching gas, and plasma is generated by giving RF (13.56 MHz) power of 500 W to a coiled electrode at a pressure of 1 Pa. RF (13.56 MHz) power of 50 W is also given to the substrate side (sample stage) so that a self-bias voltage lowers than that of the first etching treatment can be applied. The tungsten film is subjected to anisotropic etching under these conditions so that the tantalum nitride film or the titanium film serving as the first conductive layers is remained. In this way, second shape conductive layers 342 to 344 (first conductive films 342a to 344a and second conductive films 342b to 344b) are formed. Denoted by 345 is a gate insulating film and a region of the gate insulating film which is not covered with the second shape conductive layers 342 to 344 is further etched and thinned by about 20 to 50 nm.

[0095]

Then first doping treatment is performed. In this doping treatment, the film is doped with an n type impurity (donor) to form LDD regions of the n-channel TFT. The

doping is made by ion doping or ion implantation. For example, ion doping is employed and the acceleration voltage is set to 70 to 120 keV while the dose is set to 1 x 10^{13} /cm^2 to form first impurity regions. When the film is doped, the second conductive films 342b to 344b are used as masks against the impurity element and regions under the first conductive films 342a to 344a are doped with the impurity element. In this way, first impurity regions 346 to 348 are formed to partially overlap the first conductive films 342a to 344a, respectively. The first impurity regions contain the impurity element in a concentration of 1 x 10^{17} to 1 x 10^{19} /cm^3.

[0096]

Next, masks 349 to 351 are formed from a resist as shown in Fig. 12D to conduct second doping treatment. In the second doping treatment, an n type impurity (donor) is used to form a source or drain region of the n-channel TFT. Ion doping is employed and the dose is set to 1 x 10^{13} to 5 x 10^{14} /cm^2. Used as the n type impurity element is an element belonging to Group 15, typically phosphorus (P) or arsenic (As). The resist masks 349 to 351 can have their respective shapes optimized. By shaping the resist masks so as to extend over the ends of the second shape conductive layers and overlap the first impurity regions previously formed, the LDD regions can be obtained. Second impurity regions 352 to 354 are thus formed. The phosphorus (P) concentration in the second impurity regions 725 to 729 is set to 1 x 10^{20} to 1 x 10^{21} /cm^3.

[0097]

Then a resist mask 355 is formed as shown in Fig. 12E so that the island-like semiconductor layer 331 for forming the p-channel TFT is doped with a p type impurity (acceptor). Typically, boron (B) is used. The impurity concentration in third impurity regions 356, 357 is set to 2 x 10^{20} to 2 x 10^{21} /cm^3. Thus the regions are doped with boron in a concentration 1.5 to 3 times higher than the concentration of phosphorus that has been

contained, thereby inverting the conductivity type of the regions.

[00098]

The impurity regions are formed in the respective island-like semiconductor layers through the above steps. The second shape conductive layers 342 to 344 form gate electrodes. Thereafter, as shown in Fig. 12F, a protective insulating film 358 is formed from a silicon nitride film or a silicon oxynitride film by plasma CVD. The impurity elements used to dope the island-like semiconductor layers are then activated for controlling the conductivity type. The activation is preferably made by thermal annealing that uses an annealing furnace. Laser annealing or rapid thermal annealing (RTA) may be employed instead. Thermal annealing is conducted in a nitrogen atmosphere having an oxygen concentration of 1 ppm or less, preferably 0.1 ppm or less, at 400 to 700°C, typically 400 to 600°C. In this embodiment, the film is subjected to heat treatment at 500°C for four hours.

[0099]

A silicon nitride film 359 is formed and subjected to heat treatment at 350 to 450°C, preferably 410°C. At this temperature, hydrogen is released from the first interlayer insulating film. Thereafter, another heat treatment is performed at 250 to 350°C, lasting about 0.1 to 1 hour to hydrogenate the crystalline semiconductor film. Hydrogenating the crystalline semiconductor film through two-step heat treatment as above makes it possible to hydrogenate and compensate dangling bonds (uncoupled bonds) of germanium, which is difficult to hydrogenate especially at a temperature of 350°C or higher.

[0100]

An interlayer insulating film 360 is formed of an organic insulating material such as polyimide and acrylic in order to level the surface. A silicon oxide film formed by plasma CVD using TEOS (Tetraethyl Ortho Silicate) may of course be adopted instead, but

it is desirable to choose the above organic insulating material from the viewpoint of better levelness.

[0101]

Contact holes are formed next, so that source or drain wiring lines 361 to 366 are formed from aluminum (Al), titanium (Ti), tantalum (Ta) or the like.

[0102]

A p-channel TFT 370 has a channel formation region 363, and has the third impurity region 356 that function as source region or drain region. An n-channel TFT 371 has a channel formation region 368; the first impurity region 362 overlapping the gate electrode that is formed of the second shape conductive layer 343; and the first impurity region 353 functioning as a source region or a drain region. An n-channel TFT 372 has a channel formation region 369; the first impurity region 348a overlapping the gate electrode that is formed of the second shape conductive layer 344; the second impurity region 348b formed outside the gate electrode; and the first impurity region 353 functioning as a source region or a drain region. The first impurity regions 362, 348a are LDD regions overlapping gate electrodes, and are effective in easing high electric field regions formed on the drain ends to prevent degradation of TFTs due to hot carriers. The first impurity region 348b is an LDD region and, according to the process shown in this embodiment, can have dimensions optimum for reducing OFF current value.

[0103]

Through the above steps, a CMOS type TFT in which an n-channel TFT and a p-channel TFT are combined complementarily can be obtained. The process shown in this embodiment allows designing LDD regions while considering the characteristics required for the respective TFTs, so that TFTs having their respective optimum structures are formed on the same substrate. The CMOS type TFT as such can be used to form a driver circuit of

an active matrix liquid crystal display device or EL display device. Other than this use, the n-channel TFT or the p-channel TFT as above can be applied to a transistor constituting a pixel portion. The TFT may also be used as a TFT constituting a thin film integrated circuit that is to replace the conventional LSI formed from a semiconductor substrate. Although the TFT shown here has a single gate structure, the TFT may of course take a multi-gate structure in which a plurality of gate electrodes are provided.

[0104]

Using the CMOS circuit of this embodiment in combination, a basic logic circuit or a more intricate logic circuit (such as a signal divider circuit, a D/A converter, an operation amplifier and a γ correction circuit) can be formed. It also can constitute a memory or a microprocessor.

[0105]

[Embodiment 7]

This embodiment gives a description on an example of the structure of a monolithic liquid crystal display device with reference to Figs. 13 and 14. A monolithic liquid crystal display device is a device in which a pixel portion and a driver circuit are formed on the same substrate. A crystalline semiconductor film of the present invention which is comprised of silicon and germanium is used to form an active region of a switching TFT for the pixel portion and active regions of n-channel and p-channel TFTs for the driver circuit. The crystalline semiconductor film comprised of silicon and germanium may be any one of the crystalline semiconductor films formed in accordance with the methods of Embodiments 1 through 3.

[0106]

A substrate 401 in Fig. 13 is preferably a glass substrate such as barium borosilicate glass substrate or an aluminoborosilicate glass substrate. A quartz substrate

may be used instead. When the substrate 401 is a glass substrate, a blocking layer 402 is formed.

[0107]

The structure is not limited for the n-channel TFT 442 of the pixel portion 445 and for an n-channel TFT 441 and a p-channel TFT 440 of a driver circuit 444. This embodiment employs as the basic structure a TFT formed in accordance with Embodiment 6. Needless to say, a TFT according to Embodiment 4 or a TFT according to Embodiment 5 may also be employed.

[0108]

In the driver circuit 444, wiring lines 408, 417, and source or drain wiring lines 418 to 421 are formed. In the pixel portion 445, a pixel electrode 424, a gate wiring line 423, a connection electrode 422 and a source wiring line 409 are formed.

[0109]

The p-channel TFT 440 of the driver circuit 444 has, in a semiconductor layer 403, a channel formation region 426 and a third impurity region 427 that functions as a source region or a drain region. The third impurity region is formed outside a gate electrode 410 (at a position where the region does not overlap the gate electrode). The p-channel TFT structured as above is obtained by removing the resist masks after the step of Fig. 12D to selectively etch the first conductive film, and then doping the film with a p-type impurity element.

[0110]

The n-channel TFT 441 has, in a semiconductor layer 404, a channel formation region 428; a first impurity region 429 overlapping a gate electrode that is formed of a second shape conductive layer 411; and a second impurity region 430 functioning as a source region or a drain region. The n-channel TFT 441 can be fabricated in the same way

as the n-channel TFT 371 of Embodiment 6.

[0111]

The n-channel TFT 442 of the pixel portion has, in a semiconductor layer 405, a channel formation region 431; a first impurity region 432 (LDD region) formed outside a gate electrode; and second impurity regions 433, 434 and 435 functioning as source regions or drain regions. The n-channel type TFT structured as above is obtained by removing the resist masks after the step of Fig. 12D to selectively etch the first conductive film. However, in order to maintain the structure of the n-channel type TFT 441, a protective resist layer has to be formed and one more photo mask is required to form the protective resist layer.

[0112]

A semiconductor layer 406 functions as one of electrodes of a capacitor storage 443, and has a sixth impurity region 437, a fifth impurity region 438, and a region 436 that is not doped with an impurity.

[0113]

In the pixel portion 445, the source wiring line 409 is electrically connected through the connection electrode 422 to the source or drain region 433 of the pixel TFT 442. The gate wiring line 423 is electrically connected to the third shape conductive layer 412 that functions as a gate electrode. The pixel electrode 424 is connected to the source or drain region 435 of the pixel TFT 442 and to the impurity region 438 of the semiconductor film 406 that is one of electrodes of the capacitor storage 443.

[0114]

The sectional view of the pixel portion 445 in Fig. 7 is taken along the line A-A' in Fig. 14. The third shape conductive layer 412 functioning as a gate electrode doubles as one of electrodes of a capacitor storage of an adjacent pixel, and partially overlaps a

semiconductor layer 453 that is connected to a pixel electrode 452 to form a capacitance. The source wiring line 407, the pixel electrode 424 and an adjacent pixel electrode 451 are arranged such that the ends of the pixel electrodes 424, 451 are placed on the source wiring line 407 to form an overlapping portion. The overlapping portion blocks stray light and enhances light-shielding property of the device.

[0115]

[Embodiment 8]

This embodiment gives an example of manufacturing an active matrix type liquid crystal display device from the TFTs fabricated in Embodiment 7. In Fig. 15, a pixel electrode 601 is formed from a transparent conductive film on the interlayer insulating film of the pixel portion 445. The pixel electrode is connected to an auxiliary electrode 609 that is connected to the n-channel type TFT 442 of the pixel portion. The pixel electrode is also connected to an auxiliary electrode 610 of the capacitor storage 443. These auxiliary electrodes, a gate line 608, a connection electrode 607, source or drain wiring lines 603 to 606 of the TFTs of the driver circuit 444, and a wiring line 602 are obtained by forming organic resin films 611 to 619 from photoresist, photosensitive polyimide, photosensitive acrylic or the like as masks and by etching the conductive films under the masks.

[0116]

The organic resin films 611 to 619 are formed by applying an organic resin material to the entire surface of the conductive film for forming a wiring line and then patterned by light exposure process as shown in Fig. 27. Thereafter, a polyimide resin layer having a viscosity of 5 to 20 mPa is formed by offset printing, and is baked at 200°C to form an oriented film. The polyimide resin applied by offset printing can reach into the stepped portions between the organic resin films 611 to 619 and the wiring lines or electrodes under the organic resin films during baking, and covers the ends thereof. Then

the oriented film is subjected to rubbing to orient a liquid crystal.

[0117]

An opposite substrate 621 has an opposite electrode 622 that is formed of a transparent conductive film, and has an oriented film 623. The opposite substrate 621 is bonded, using a sealing member 624, to a substrate on which the pixel portion 445 and the driver circuit 444 are formed. The sealing member 624 has a filler (not shown in the drawing) mixed therein. The filler, together with a spacer (not shown in the drawing), keeps the distance between the substrates uniform when the substrates are bonded to each other. Thereafter, a liquid crystal 625 is injected between the substrates. A known liquid crystal material can be used. For example, a thresholdless antiferroelectric liquid crystal mixture can be used as well as a TN liquid crystal. The thresholdless antiferroelectric liquid crystal mixture exhibits electro-optical responsiveness in which the transmittance changes continuously in relation to the electric field. Some of antiferroelectric liquid crystal mixtures exhibit an electro-optical response characteristic that forms a letter V when graphed. In this way, an active matrix liquid crystal display device shown in Fig. 27 is completed.

[0118]

[Embodiment 9]

The description given below with reference to Fig. 17 is about an example of manufacturing a display device utilizing electroluminescence (EL) from TFTs fabricated in accordance with Embodiments 4 through 6.

[0119]

Fig. 27 shows an example of a light emitting device in which a pixel portion and a driver circuit for driving the pixel portion are formed on the same insulator (the device shown is not sealed yet). A CMOS circuit that is the basic unit is shown as the driver

circuit and only one pixel is shown as the pixel portion. This CMOS circuit is obtained in accordance with Embodiment 6.

[0120]

In Fig. 17, a substrate 700 is an insulator and an n-channel type TFT 701, a p-channel type TFT 702, a switching TFT 703 that is from a p-channel type TFT; and a current controlling TFT 704 that is from an n-channel type TFT are formed on it. Channel formation regions of these TFTs are formed of a crystalline semiconductor film that is formed in accordance with the present invention. Specifics of the formation method are described in Embodiments 1 through 3.

[0121]

The n-channel type TFT 701 and the p-channel type TFT 702 are as described in Embodiment 6 and hence the explanations thereof are omitted here. The switching TFT 703 has a structure in which two channel formation regions are formed between a source region and a drain region (double gate structure). This embodiment is not limited to the double gate structure but may take the single gate structure in which one channel formation region is formed or the triple gate structure in which three channel formation regions are formed.

[0122]

A contact hole is formed in a first interlayer insulating film 706 on a drain region 705 of the current controlling TFT 704 before a second interlayer insulating film 707 is formed. This is to facilitate the etching process when a contact hole is formed in the second interlayer insulating film 707. The contact hole formed in the second interlayer insulating film 707 reaches the drain region 705, and a pixel electrode 708 connected to the drain region 705 is provided. The pixel electrode 708 is an electrode functioning as a cathode of an EL element, and is formed of a conductive film containing an element that

belongs to Group 1 or 2 in the periodic table. In this embodiment, a conductive film of a compound of lithium and aluminum is used.

[0123]

Denoted by 713 is an insulating film formed to cover the end of the pixel electrode 708, and the insulating film is called herein as a bank. The bank 713 may be an insulating film containing silicon or a resin film. When a resin film is used, carbon particles or metal particles are put in the resin film so that the resistivity of the resin film is changed to 1×10^6 to 1×10^{12} Ωm (preferably 1×10^8 to 1×10^{10} Ωm). This prevents dielectric breakdown upon film formation.

[0124]

An EL element 709 is composed of the pixel electrode (cathode) 708, an EL layer 711 and an anode 712. The anode 712 is formed of a conductive film having a large work function, typically, an oxide conductive film. An indium oxide film, a tin oxide film, a zinc oxide film, and a compound film of these oxides may be used. The EL layer in this specification refers to a laminate obtained by combining a light emitting layer with a hole injection layer, a hole transportation layer, a hole blocking layer, an electron transportation layer, an electron injection layer, or an electron blocking layer.

[0125]

Though not shown, it is effective to form a passivation film so as to cover the EL element 709 completely after the anode 712 is formed. For the passivation film, an insulating film such as a carbon film, a silicon nitride film, and a silicon oxynitride film is formed. The passivation film may be a single layer or laminate of these insulating films.

[0126]

[Embodiment 10]

The semiconductor device of the present invention can be applied to the circuits

to substitute for the display devices and integrated circuits of a variety of electronic devices and to substitute for the conventional integrated circuits. Such semiconductor devices include portable data terminals (electronic notebook, mobile computer, cell phone, etc.), video camera, still camera, personal computer, TV and projector. Their examples are shown in Figs. 22 to 24.

[0127]

Fig. 22A shows a cell phone which comprises a display panel 2701, an operation panel 2702 and a connection portion 2703, the display panel 2701 including a display device 2704 typified by a liquid crystal display device or an EL display device, a voice output unit 2705 and an antenna 2709. The operation panel 2702 includes operation keys 2706, a power source switch 2702, a voice input unit 27058, and so on. This invention forms the display device 2904 and the semiconductor integrated circuit which accompanies it.

[0128]

Fig. 22B shows a video camera which comprises a main body 9101, a display device 9102 typified by a liquid crystal display device or an EL display device, a voice input unit 9103, operation switches 9104, a battery 9105 and an image receiving unit 9106. The invention can be applied to the display device 9102 and the semiconductor integrated circuit which accompanies it.

[0129]

Fig. 22C shows a mobile computer or a portable data terminal which is constituted by a main body 9201, a camera unit 9202, a picture unit 9203, operation switches 9204 and a display device 9205 typified by a liquid crystal display device or an EL display device. The semiconductor device of this invention can be applied to the display device 9205 and the semiconductor integrated circuit which accompanies it.

[0130]

Fig. 22D shows a TV receiver constituted by a main body 9401, a speaker 9402, a display device 9403 typified by a liquid crystal display device or an EL display device, a receiver unit 9404 and an amplifier unit 9405. The invention can be applied to the display device 9403 and the semiconductor integrated circuit which accompanies it.

[0131]

Fig. 22E shows a portable notebook constituted by a main body 9501, display devices 9502, 9503 typified by a liquid crystal display device or an EL display device, a storage medium 9504, operation switches 9505 and an antenna 9506, which is used for displaying data stored in a mini-disk (MD) or in a DVD and for displaying data received by the antenna. The invention can be applied to the display devices 9502, 9503 and to the storage medium 9504 and the semiconductor integrated circuit which accompanies it.

[0132]

Fig. 23A shows a personal computer constituted by a main body 9601, an image input unit 9602, a display device 9603 typified by a liquid crystal display device or an EL display device and a keyboard 9604. The invention can be applied to the display device 9601 and to various integrated circuits contained therein.

[0133]

Fig. 23B shows a player using a recording medium recording a program (hereinafter referred to as recording medium), which is constituted by a main body 9701, a display device 9702 typified by a liquid crystal display device or an EL display device, a speaker unit 9703, a recording medium 9704 and operation switches 9705. This device uses a DVD (Digital Versatile Disc) or a CD as a recording medium, with which the user can enjoy appreciating music, movies, or playing games or Internet. The invention can be

applied to the display device 9702 and to various integrated circuits contained therein.

[0134]

Fig. 23C shows a digital camera constituted by a main body 9801, a display device 9802 typified by a liquid crystal display device or an EL display device, an eyepiece unit 9803, operation switches 9804 and an image receiving unit (not shown). The invention can be applied to the display device 9802 and to various integrated circuits contained therein.

[0135]

Fig. 24A shows a front-type projector constituted by a projector 3601 and a screen 3602. The invention can be applied to the projector 3601 and to other signal control circuits.

[0136]

Fig. 24B shows a rear-type projector constituted by a main body 3701, a projector 3702, a mirror 3703 and a screen 3704. The invention can be applied to the projector 3702 and other signal control circuits.

[0137]

Fig. 24C is a diagram illustrating an example of structures of the projectors 3601, 3702 in Figs. 24A and 24B. The projectors 3601, 3702 are constituted by an optical system 3801 of a source of light, mirrors 3802, 3804 to 3806, a dichroic mirror 3803, a prism 3807, a liquid crystal display device 3808, a phase difference plate 3809 and a projection optical system 3810. The projection optical system 3810 is constituted by an optical system inclusive of a projection lens. Though this embodiment shows an example of the three-plate type, there may be employed the one of the single-plate type without being limited thereto. In the optical paths indicated by arrows in Fig. 24C, further, the user may

suitably provide an optical system such as an optical lens, a film having a polarizing function, a film for adjusting the phase difference or an IR film.

[0138]

Fig. 24D is a diagram illustrating an example of the structure of the optical system 3801 of the source of light in Fig. 24C. In this embodiment, the optical system 3801 of the source of light is constituted by a reflector 3811, a source of light 3812, lens arrays 3813, 3814, a polarizer/converter element 3815 and a focusing lens 3816. The optical system of the source of light shown in Fig. 24D is only an example, and is not particularly limited thereto only. For example, the user may suitably provide the optical system of the source of light with an optical system such as an optical lens, a film having a polarizing function, a film for adjusting the phase difference or an IR film.

[0139]

Though not diagramed, the invention can be further applied as a display device to navigation systems as well as to refrigerators, washing machines, microwave ovens, fixed telephones and display device integrated facsimile. Thus, the invention has a very wide range of applications and can be applied to a variety of products.

[0140]

[Effect of the Invention]

As described above, an active region of a semiconductor device can be formed by using a crystalline semiconductor film of the present invention. It is especially suitable for a channel formation region of a thin film transistor. A TFT formed from this crystalline semiconductor film can be used as a TFT for manufacturing an active matrix liquid crystal display device or EL display device, or as a TFT constituting a thin film integrated circuit that is to replace the conventional LSI formed on a semiconductor substrate.

[Brief Description of the Drawings]

[Fig. 1] A graph containing data for orientation ratio of a crystalline semiconductor film, showing duty ratio dependency in intermittent electric discharge as a film formation condition of an early deposition film

[Fig. 2] A graph containing data for orientation ratio of a crystalline semiconductor film, showing electric discharge duration dependency in intermittent electric discharge as a film formation condition of an early deposition film

[Fig. 3] A graph containing data for orientation ratio of a crystalline semiconductor film, showing repetition frequency dependency in intermittent electric discharge as a film formation condition of an early deposition film

[Fig. 4] A diagram showing the structure of a plasma CVD apparatus used in the present invention

[Fig. 5] A diagram showing the structure of a reaction chamber of the plasma CVD apparatus used in the present invention

[Fig. 6] Schematic diagrams showing examples of reverse pole diagrams obtained by an EBSP method

[Fig. 7] Diagrams illustrating a method of forming a crystalline semiconductor film according to the present invention

[Fig. 8] Diagrams illustrating a method of forming a crystalline semiconductor film according to the present invention

[Fig. 9] Diagrams illustrating a method of forming a crystalline semiconductor film according to the present invention

[Fig. 10] A sectional view illustrating the structure of a reverse stagger TFT using a crystalline semiconductor film of the present invention

[Fig. 11] Diagrams illustrating a process of manufacturing a TFT using a crystalline

semiconductor film according to the present invention

[Fig. 12] Diagrams illustrating a process of manufacturing a TFT with a CMOS structure from a crystalline semiconductor film according to the present invention

[Fig. 13] A sectional view illustrating the structure of a display device using a crystalline semiconductor film according to the present invention

[Fig. 14] A top view of a pixel structure in a pixel portion

[Fig. 15] A sectional view illustrating the structure of a liquid crystal display device using a crystalline semiconductor film according to the present invention

[Fig. 16] A sectional view illustrating the structure of an EL display device formed from a crystalline semiconductor film according to the present invention

[Fig. 17] Pictures taken during oscilloscope observation of the waveform of high frequency power applied to a cathode in intermittent electric discharge plasma CVD

[Fig. 18] A diagram of a model for explaining application of high frequency power and a generation process of radicals

[Fig. 19] A diagram illustrating a crystallization model in which $NiSi_x$ serves as a nuclear

[Fig. 20] Cumulative frequency graphs showing the distance between adjacent crystal nuclei

[Fig. 21] A graph showing the relation between the flow rate of GeH_4 and crystal nuclear generation density

[Fig. 22] Diagrams showing examples of semiconductor device

[Fig. 23] Diagrams showing examples of semiconductor device

[Fig. 24] Diagrams showing examples of projector